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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KANG, DONGHEE	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,476	CANTELL ET AL.	
	Examin r	Art Unit	
	Donghee Kang	2811	

-- The MAILING DATE of this communication appears on the cov r sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 22-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 22-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Acknowledgment

1. Applicant's Amendment and Response to Paper No.4 have been entered and made of Record (Paper No.5). Claims 17-21 are cancelled and new claims 22-34 are added. Thus claims 1-16 & 22-34 are pending in this application.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim **25** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claim 25 is incomplete because of missing a further limitation (e.g., comprising the steps of:)

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims **1, 4-6, 8-11, 13-16 & 22** are rejected under 35 U.S.C. 102(b) as being anticipated by Fitch et al. (US 5,213,989).

Re claim **1**, Fitch et al. teach a method for forming a transistor, the method comprising the steps of:

providing a semiconductor substrate (12, Fig.7); forming an epitaxial layer (18, Fig.7:Col.3, lines 8-11); forming a dopant source layer (50, Fig.9) on the epitaxial layer; and diffusing dopant from the dopant source layer into the epitaxial layer to form at least a portion of an extrinsic base (52, Fig.10) for the transistor within the epitaxial layer, said portion of the extrinsic base being in direct mechanical contact with the dopant source layer, said portion of the extrinsic base being disposed between the dopant source layer (50) and an intrinsic base (44) for the transistor, said intrinsic base being totally within the epitaxial layer (18).

Re claims **4 & 15**, Fitch et al. teach the method further comprising the step of implanting into the epitaxial layer, the implanting forming a second portion of the extrinsic base for the transistor (Col.5, line 65 - Col.6, line 2).

Re claim **5**, Fitch et al. teach the method further comprising the step of forming a pedestal (22, 40, & 42: Fig.8) on the epitaxial layer, and wherein the dopant source layer (50:Fig.9) is formed around the such that the pedestal defines a portion of the epitaxial layer in which the dopant source layer is not formed on the epitaxial layer.

Re claim **6**, Fitch et al. teach the pedestal further defines an emitter opening (Fig.11).

Re claims **8 & 13**, Fitch et al. teach the step of forming a pedestal comprises depositing and patterning an oxide layer (Figs. 7 & 8).

Re claims **9 & 14**, Fitch et al. teach the dopant source layer comprises a raised portion of the extrinsic base.

Re claim **10**, Fitch et al. teach a method for forming bipolar transistor on a semiconductor substrate, the method comprising the steps of (Figs.7-12):

providing a semiconductor substrate (12); forming an epitaxial layer (18) on the semiconductor substrate; forming a pedestal (22,44,&42:Fig.7) on epitaxial layer, the pedestal defining an emitter region of the epitaxial layer (Fig.11); forming a dopant source layer (50) on the epitaxial layer, the dopant source layer not formed on the epitaxial layer where the pedestal is on the epitaxial layer; and diffusing dopant from the dopant source layer into the epitaxial layer to form at least a portion of an extrinsic base (Col.7, lines 3-6) for the transistor within the epitaxial layer, said portion of the extrinsic base being in direct mechanical contact with the dopant source layer, said portion of the extrinsic base being disposed between the dopant source layer and an intrinsic base for the transistor, said intrinsic base being totally within the epitaxial layer.

Re claim **11**, Fitch et al. the epitaxial layer comprises silicon germanium (Col.3, lines 6-11 &Col.2, lines 61-65).

Reclaim **16**, Fitch et al. teach the dopant source layer is self-aligned to the pedestal.

Re claim **22**, Fitch et al. teach a method for forming bipolar transistor on a semiconductor substrate, the method comprising the steps of (Figs.7-12):

providing a semiconductor substrate (12); forming an epitaxial layer (18) on the semiconductor substrate; forming a dopant source layer (50) on a first portion of the epitaxial layer; forming an emitter material (60, Fig.11) on a second portion of the epitaxial layer, said second portion of the epitaxial layer being adjacent to said first

portion of the epitaxial layer; diffusing dopant from the dopant source layer into the epitaxial layer to form at least a portion of an extrinsic base (Col.7, lines 3-6) for the transistor within the epitaxial layer, said portion of the extrinsic base being in direct mechanical contact with the dopant source layer, said portion of the extrinsic base being disposed between the dopant source layer and an intrinsic base for the transistor, said intrinsic base being totally within the epitaxial layer; and diffusing emitter dopant from the emitter material into said second portion of the epitaxiaal layer, said emitter dopant diffusion forming an emitter (58) for the transistor, said emitter being totally within the epitaxial layer, said emitter being surround by said portion of the extrinsic base.

6. Claims **22-24** are rejected under 35 U.S.C. 102(b) as being anticipated by Jang (US 6,177,325).

Re claim **22**, Jang teaches a method for forming bipolar transistor on a semiconductor substrate, the method comprising the steps of:

providing a semiconductor substrate (112, Fig.6); forming an epitaxial layer (116) on the semiconductor substrate; forming a dopant source layer (13-, Fig.7) on a first portion of the epitaxial layer; forming an emitter material (131, Fig.10) on a second portion of the epitaxial layer, said second portion of the epitaxial layer being adjacent to said first portion of the epitaxial layer; diffusing dopant from the dopant source layer into the epitaxial layer to form at least a portion of an extrinsic base (124, Fig.11: Col.4, line 66-Col.5, line1) for the transistor within the epitaxial layer, said portion of the extrinsic base being in direct mechanical contact with the dopant source layer, said portion of the

extrinsic base being disposed between the dopant source layer and an intrinsic base (122) for the transistor, said intrinsic base being totally within the epitaxial layer; and diffusing emitter dopant from the emitter material into said second portion of the epitaxiaal layer, said emitter dopant diffusion forming an emitter (129) for the transistor, said emitter being totally within the epitaxial layer, said emitter being surround by said portion of the extrinsic base.

Re claim **23**, Jang teaches the step of diffusing emitter dopant from the emitter material is performed concurrent with the step of diffusing dopant from the dopant source layer (Col.4, line 66-Col.5, line 1).

Re claim **24**, Jang teaches the step of diffusing emitter dopant from the emitter material and step of diffusing dopant from the dopant source layer are performed by an annealing process.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim **2** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fitch et al. (US 5,213,989).

Fitch et al. teach the dopant source layer, which also serves as a base electrode, comprising an epitaxially grown conductive layer but do not teach a doped single crystal

layer. In alternative embodiment, however, Fitch et al. note that the dopant source can be polysilicon, amorphous silicon or a like silicon-based material (Col.3, lines 52-54).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the doped single crystal silicon layer as the dopant source in Fitch's device, since the single crystal silicon layer has a higher electron mobility than polycrystal silicon hence serving as a better base electrode.

9. Claim **3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fitch et al. in view of Johnson (US 5,592,017).

Fitch et al. do not teach the dopant source layer is doped between 5×10^{19} and 1×10^{21} atoms/cm^3. However, Johnson teaches the dopant source is doped atoms/5×10^{19} cm^3 which is in the claimed ranges (Col.4, lines 14-16). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the dopant concentration at 5×10^{19} atoms/cm^3 as taught by Johnson in the Fitch's device in order to provide enough diffusion dopant species into the epitaxial layer to form extrinsic base layer.

Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the concentration of the layer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

10. Claims **7 & 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fitch et al. and in view of Ozkan et al. (US 6,437,376).

Fitch et al. teach the step of forming a pedestral comprises forming silicon dioxide (22), a nitride layer (40), and an oxide layer (42), and patterning the silicon dioxide, nitride layer and oxide layer (Figs. 7 & 8). However, Fitch et al. do not teach the silicon dioxide is high pressure oxide layer (HIPOX). Ozkan teaches forming high pressure oxide layer (132, Fig. 10) on the SiGe layer. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form oxide layer under high pressure as taught by Ozkan in Fitch's device, since HIPOX layer is wet etched by a quick HF dip so that the emitter windows reveals SiGe base without damage.

11. Claims **26-34** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fitch et al. (US 5,213,989) in view of Sato (US 6,436,781).

Re claims **26, 29 & 32**, Fitech et al. do not teach forming a pedestal implant within the semiconductor substrate. Sato in Fig.1 teaches forming the pedestal implant (9 & 12), wherein the pedestal implant has a first surface and an opposing second surface, wherein the first surface of the pedestal implant is in direct mechanical contact with the subcollector (2a), wherein the second surface of the pedestal implant is in direct mechanical contact with the intrinsic base (11), and wherein the pedestal implant is not in direct mechanical contact with said portion of the extrinsic base. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was

made to incorporate the teaching of Sato into Fitch's device in order to reduce the parasitic capacitiance.

Re claims **27, 30, 33**, Sato teaches the step of forming the subcollector is performed before the step of forming the pedestal implant.

Re claims **28, 31 & 34**, Sato teach the method further comprising: forming deep trench isolation at the edge of the subcollector, said deep trench usolation surrounding the subcollector and electrically isolating the subcollector.

Allowable Subject Matter

12. Claim 25 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Prior art reference, taken along or in combination, do not teach or render obvious that the method further comprising the steps of:

Providing a cap layer on the dopant source; and providing a spacer layer on the cap layer, wherein a first surface of the spacer layer is in direct mechanical contact with a first surface of the cap layer, wherein a second surface of the cap layer is in direct mechanical contact with a surface of the dopant source layer.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 703-305-9147. The examiner can normally be reached on Maxiflex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on 703-308-1690. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Donghee Kang
Examiner
Art Unit 2811

dhk